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SERIAL NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
08/480,738	06/07/95	ZURAVL FEF	W 018414-133

<p>JAMES A LABARRE BURNS DOANE SWECKER & MATHIS P O BOX 1404 ALEXANDRIA VA 22313-1404</p>	<p>B3M1/0920</p>
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PHAN, REXAMINER	
ART UNIT	PAPER NUMBER
2305	3

DATE MAILED: 09/20/96

Please find below a communication from the EXAMINER in charge of this application.

SEE THE ATTACHED ACTION

Commissioner of Patents

Office Action Summary

Application No.

08/480,738

Applicant(s)

Zuravleff et al.

Examiner

Raymond N. Phan

Group Art Unit

2305



☐ Responsive to communication(s) filed on _____

☐ This action is FINAL.

☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) 1-38 is/are pending in the application.

Of the above, claim(s) 27-34 is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 1-26 and 35-38 is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been
☐ received.

☐ received in Application No. (Series Code/Serial Number) _____

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892 ✓

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 2 ✓

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

Part III DETAILED ACTION

Notice to Applicant(s)

1. This application has been examined. Claims 1-38 are pending.
2. The Group and/or Art Unit location of your application in the PTO has changed. To aid in correlating any papers for this application, all further correspondence regarding this application should be directed to Group Art Unit 2305.

Election/Restriction

3. Restriction to one of the following inventions is required under 35 U.S.C. 121:

Group I. Claims 1-26 and 35-38 are, drawn to dual bus system, classified in Class 395, subclass 308.

Group II. Claims 27-34 are, drawn to the buffer for a multiprocessor system running real time processes, classified in Class 395, subclass 250.

The inventions are distinct, each from the other because of the following reasons:

4. Inventions I and II are related as subcombinations disclosed as usable together in a single combination. Inventions in this relationship are distinct from each other if they are shown in a single combination. See (M.P.E.P. § 806.05(c)). In the instant case, invention I has separate utility such as in the

systems that do not employ the use of a multi-processor system running real time processes.

5. Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

6. During a telephone conversation with Mr. Mark Superko (Reg. # 34,027) on August 19, 1996 a provisional election was made with traverse to prosecute the invention of Group I, claims 1-26 and 35-38. Affirmation of this election must be made by applicant in responding to this Office action. Claims 27-34 are withdrawn from further consideration by the Examiner, 37 C.F.R. § 1.142(b), as being drawn to a non-elected invention.

7. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 C.F.R. § 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a diligently-filed petition under 37 C.F.R. § 1.48(b) and by the fee required under 37 C.F.R. § 1.17(h).

Drawings

8. The drawings submitted with this application were declared informal by the applicant which are acceptable for examination purpose only. Accordingly they

have not been reviewed by a draftperson at this time. When formal drawings are submitted, the draftperson will perform a review. Formal drawings will be required when the application is allowed.

9. Direct any inquiries concerning drawing review to the Drawing Review Branch (703) 305-8404.

Specification

10. The following is a quotation of the first paragraph of 35 U.S.C. § 112:
The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

The specification is objected to under 35 U.S.C. § 112, first paragraph, as failing to teach how each of the caches corresponds to each of the processors.

The disclosure is non-enabling for claims 16 and 26 because the limitations recited in the claims 16 and 26 were merely hinted as possible modifications to the claimed invention and no circuit diagrams or suggestion were provided to make modifications as hinted. Therefore, undue experimentation is required and the disclosure does not enable a person skilled in the art to make and use the claimed invention.

Claim Rejections - 35 USC § 112

11. Claims 16 and 26 are rejected under 35 U.S.C. § 112, first paragraph, for the reasons set forth in the objection to the specification.

Claim Rejections - 35 USC § 102

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

13. Claims 1-11, 14-15, 17-20, and 35-38 are rejected under 35 U.S.C. § 102(e) as being anticipated by Bell et al. (US No. 5,546,546).

In regards to claims 1 and 4, Bell et al. disclose a bus bridge for maintaining the transactions ordering between the processor-memory bus and I/O bus (abstract). Moreover, Bell et al. teach the bus bridge holding the data requests so that the plurality of I/O transactions may be performed simultaneously (see col. 2, lines 55-67; col. 3, lines 1-23). Furthermore, Bell et al. inherently teach the speed of processor-memory bus and I/O bus.

In regards of claims 2-3, Bell et al. teach the I/O transactions comprising loads and stores (see col. 6, lines 38-67; col. 7, lines 1-46).

In regards to claim 5, Bell et al. teach the processor-memory bus connected to a plurality of processors and a caching unit (see col. 4, lines 35-59).

In regards to claim 6, Bell et al. teach the I/O bus connected to the plurality of peripheral devices (see col. 5, lines 5-35).

In regards to claims 7-8, Bell et al. teach the bus bridge comprising a control block (i.e. transaction arbitration unit), and plurality memory arrays (see abstract and col. 8, lines 20-37).

In regards to claim 9, Bell et al. teach that the transaction arbitration unit comprises the plurality of inbound/outbound queues and data pools (see col. 9, lines 30-67; col. 10, lines 1-5).

In regards to claim 10, Bell et al. teach that the plurality of queues comprise a pending queue corresponding to each of the plurality of peripheral devices connected to the I/O bus (see col. 9, lines 53-61).

In regards to claim 11, Bell et al. teach that the bus bridge holds the transactions of data requests and I/O data in the queues and data pools (see col. 9, lines 47-67, col. 10, lines 1-5)

Claims 14-15 and 17-19 are the apparatus claims corresponding to the claim 5. Therefore, claims 14-15 and 17-19 are rejected for the same rationale set forth claim 5.

Claim 20 is the apparatus claim corresponding to the claims 1 and 5-6. Therefore, claim 20 is rejected for the same rationale set forth claims 1 and 5-6.

Claims 35-38 are the method claims corresponding to the apparatus claims 1-3. Therefore, claims 35-38 are rejected for the same rationale set forth claims 1-3.

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. § 103 which forms the basis for all obviousness rejections set forth in this Office action:

A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. § 103, the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 C.F.R. § 1.56

to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of potential 35 U.S.C. § 102(f) or (g) prior art under 35 U.S.C. § 103.

15. Claims 12-13, and 16 are rejected under 35 U.S.C. § 103 as being unpatentable over Bell et al. in view of Park et al. (US No. 5,526,508).

In regards to claim 12, Bell et al. disclose the claimed subject matter as discussed above except load addresses storing in a memory array and sent to peripheral devices and returned from the peripheral devices and stored in the memory array until the processor is ready to receive the data. However, Park et al. teach the cache line replacing apparatus which includes a first storage unit storing write data of CPU/cache bus, and a second storage unit storing read data from main memory to the memory bus (Col. 3, lines 4-42). It would simultaneously provide data transfer between two buses. Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have the teachings of Park et al. into the teachings of Bell et al. because it would prevent the time delay due to the write back buffering.

In regards to claim 13, Bell et al. teach the memory storing a address and data (see col. 8, lines 10-37).

In regards to claim 16, Bell et al. teach that each of the caches corresponds to each of the processors (see col. 4, lines 42-45).

16. Claims 21-26 are rejected under 35 U.S.C. § 103 as being unpatentable over Bell et al. in view of Amini et al. (US No. 5,542,055).

Bell et al. disclose the claimed subject matter as discussed above except the supporting of bandwidth of load buffer and peripheral bus. However, Amini

et al. teach the supporting of bandwidth of bus bridge (see col. 5, lines 22-38). It performs significant data transfer in a relatively short period of time. Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have the teachings of Amini et al. into the teachings of Bell et al. because it would provide a greater speed in data transmission.

In regards to claims 22-23, it would have been obvious that the data request must comprise an address, control information, and data in order to transfer data between two buses.

Claims 24-25 are the apparatus claims corresponding to the claim 5. Therefore, claim 24-25 are rejected for the same rationale set forth claim 5.

Claim 26 is the apparatus claim corresponding to the claim 16. Therefore, claim 26 is rejected for the same rationale set forth claim 16.

Conclusion

17. Claims 1-26 and 35-38 are rejected. Claims 27-34 have been withdrawn from consideration.

18. The prior arts made of record and not relied upon are considered pertinent to applicant's disclosure.


Bell et al. (US No. 5,535,340) disclose a method and apparatus for maintaining transaction ordering and supporting deferred replies in a bus bridge.

Amini et al. (US No. 5,499,346) disclose a bus-to-bus bridge for multiple bus information handling system that optimizes data transfers between a system bus and a peripheral bus.

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Raymond Phan, whose telephone number is (703) 306-2756. The examiner can normally be reached on Monday-Thursday from 6:30AM-4:00PM. The examiner can also be reached on alternate Fridays during the same hours.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Harvey, can be reached on (703) 305-9705. The fax phone number for this Group is (703) 308-5358.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-9600.


JACK B. HARVEY
SUPERVISORY PATENT EXAMINER
GROUP 2300

RP
Raymond Phan
September 14, 1996